AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (original): A clock signal transmitting system, comprising:

a controlling circuit for generating a first control signal and a second control signal which contains synchronization information of said first control signal;

a first reference voltage generating circuit for generating a first reference voltage which periodically varies corresponding to said first control signal;

a second reference voltage generating circuit for generating a second reference voltage which periodically varies corresponding to said second control signal;

a first comparator for comparing a source clock signal with said first reference voltage in order to generate a transmission clock signal; and

a second comparator for comparing said transmission clock signal with said second reference voltage in order to generate a reproduced clock signal.

2. (original): The clock signal transmitting system as set forth in claim 1,

wherein the sum of said first reference voltage generated by said first reference voltage generating circuit and said second reference voltage generated by said second reference voltage generating circuit is a constant voltage.

3. (original): The clock signal transmitting system as set forth in claim 1,

wherein said first reference voltage generated by said first reference voltage generating circuit and said second reference voltage generated by said second reference voltage generating circuit periodically vary in the same period.

4. (original): The clock signal transmitting system as set forth in claim 1,

wherein said first reference voltage generating circuit switches said first reference voltage at a frequency twice as high as said source clock signal, and

wherein said second reference voltage generating circuit switches said second reference voltage at the frequency twice as high as said source clock signal.

5. (original): The clock signal transmitting system as set forth in claim 1,

wherein said controlling circuit is disposed on a transmission side.

6. (original): The clock signal transmitting system as set forth in claim 5,

wherein said controlling circuit generates said first control signal and said second control signal on the basis of said source clock signal.

7. (original): The clock signal transmitting system as set forth in claim 5,

wherein said controlling circuit generates said first control signal and said second control signal on the basis of said transmission clock signal.

8. (original): The clock signal transmitting system as set forth in claim 5,

wherein said controlling circuit generates said first control signal and said second control signal on the basis of said source clock signal and said transmission clock signal.

9. (currently amended): The clock signal transmitting system as set forth in ~~claims~~claim 1,

wherein said controlling circuit generates said second control signal having a frequency which is lower than a frequency of said source clock signal.

10. (original): The clock signal transmitting system as set forth in claim 1,

wherein said first reference voltage generating circuit generates said first reference voltage on the basis of said first control signal and said source clock signal.

11. (original): The clock signal transmitting system as set forth in claim 1,

wherein said first reference voltage generating circuit generates said first reference voltage on the basis of said first control signal and said transmission clock signal.

12. (original): The clock signal transmitting system as set forth in claim 1,

wherein said second reference voltage generating circuit generates said second reference voltage on the basis of said second control signal and said transmission clock signal.

13. (currently amended): The clock signal transmitting system as set forth in ~~claims~~ claim 1,

wherein said second reference voltage generating circuit generates said second reference voltage on the basis of said second control signal and said reproduced clock signal.

14. (original): The clock signal transmitting system as set forth in claim 1, further comprising:

a local oscillator disposed on a reception side for generating a local clock signal,

wherein said second reference voltage generating circuit generates said second reference voltage on the basis of said second control signal and said local clock signal.

15. (original): The clock signal transmitting system as set forth in claim 1, further comprising:

a PLL circuit which inputs said reproduced clock signal as a reference signal in order to output a refined reproduced clock signal.

16. (original): The clock signal transmitting system as set forth in claim 1, further comprising:

a PLL circuit which inputs said reproduced clock signal as a reference signal in order to output a refined reproduced signal, wherein said second reference voltage generating circuit generates said second reference voltage on the basis of said second control signal and said refined reproduced signal.

17. (original): The clock signal transmitting system as set forth in claim 1, further comprising:

a phase compensating circuit for compensating the phase of said reproduced clock signal.

18. (original): The clock signal transmitting system as set forth in claim 1,

wherein said first control signal is the same as said second control signal.

19. (original): A digital signal transmitting system, comprising:

the clock transmitting system as set forth in claim 1;

a third comparator for comparing a source data signal with said first reference voltage in order to generate a transmission data signal; and

a fourth comparator for comparing said transmission data signal with said second reference voltage in order to generate a reproduced data signal.

20. (original): A clock signal transmitting method, comprising the steps of:

(a) generating a first control signal and a second control signal which contains synchronization information of said first control signal;

(b) generating a first reference voltage which periodically varies corresponding to said first control signal;

(c) generating a second reference voltage which periodically varies corresponding to said second control signal;

(d) comparing a source clock signal with said first reference voltage in order to generate a transmission clock signal; and

(e) comparing said transmission clock signal with said second reference voltage in order to generate a reproduced clock signal.

21. (original): The clock signal transmitting method as set forth in claim 20,

wherein the sum of said first reference voltage generated at the first reference voltage generating step (b) and said second reference voltage generated at the second reference voltage generating step (c) is a constant voltage.

22. (original): The clock signal transmitting method as set forth in claim 20,

wherein said first reference voltage generated at the first reference voltage generating step (b) and said second reference voltage generated at the second reference voltage generating step (c) periodically vary in the same period.

23. (original): The clock signal transmitting method as set forth in claim 20, wherein the first reference voltage generating step (b) is performed by switching said first reference voltage at a frequency twice as high as said source clock signal, and

wherein the second reference voltage generating step (c) is performed by switching said second reference voltage at the frequency twice as high as said source clock signal.

24. (original): The clock signal transmitting method as set forth in claim 20, wherein the first and second control signals generating step (a) is performed on a transmission side.

25. (original): The clock signal transmitting method as set forth in claim 24, wherein the first and second control signals generating step (a) is performed by generating said first control signal and said second control signal on the basis of said source clock signal.

26. (original): The clock signal transmitting method as set forth in claim 24, wherein the first and second control signals generating step (a) is performed by generating said first control signal and said second control signal on the basis of said transmission clock signal.

27. (original): The clock signal transmitting method as set forth in claim 24,

wherein the first and second control signals generating step (a) is performed by generating said first control signal and said second control signal on the basis of said source clock signal and said transmission clock signal.

28. (original): The clock signal transmitting method as set forth in claim 20,

wherein the first and second control signals generating step (a) is performed by generating said second control signal having a frequency which is lower than a frequency of said source clock signal.

29. (original): The clock signal transmitting method as set forth in claim 20,

wherein the first reference voltage generating step (b) is performed by generating said first reference voltage on the basis of said first control signal and said source clock signal.

30. (original): The clock signal transmitting method as set forth in claim 20, wherein the first reference voltage generating step (b) is performed by generating said first reference voltage on the basis of said first control signal and said transmission clock signal.

31. (original): The clock signal transmitting method as set forth in claim 20,

wherein the second reference voltage generating step (c) is performed by generating said second reference voltage on the basis of said second control signal and said transmission clock signal.

32. (original): The clock signal transmitting method as set forth in claim 20, wherein the second reference voltage generating step (c) is performed by generating said second reference voltage on the basis of said second control signal and said reproduced clock signal.

33. (original): The clock signal transmitting method as set forth in claim 20, further comprising the step of

(f) generating a local clock signal on a reception side,

wherein the second reference voltage generating step (c) is performed by generating said second reference voltage on the basis of said second control signal and said local clock signal.

34. (original): The clock signal transmitting method as set forth in claim 20, further comprising the step of:

(g) supplying said reproduced clock signal as a reference signal to a PLL circuit in order to obtain a refined reproduced clock signal from said PLL circuit.

35. (original): The clock signal transmitting method as set forth in claim 20, further comprising the step of:

(h) supplying said reproduced clock signal as a reference signal to a PLL circuit in order to obtain a refined reproduced clock signal from said PLL circuit,

wherein said second reference voltage generating step (c) is performed by generating said second reference voltage on the basis of said second control signal and said refined reproduced clock signal.

36. (original): The clock signal transmitting method as set forth in claim 20, further comprising the step of:

(i) compensating the phase of said reproduced clock signal.

37. (original): The clock signal transmitting method as set forth in claim 20, wherein said first control signal is the same as said second control signal.

38. (currently amended): A digital signal transmitting method, comprising the steps of:

the clock transmitting method as set forth in claim 20;

(j) comparing a source data signal with said first reference voltage in order to generate a transmission data signal; and

(k) comparing said transmission data signal with said second reference voltage in order to generate a reproduced data ~~signalq~~signal.